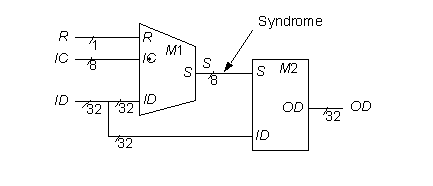
**ISCAS-85 C499/C1355 32-Bit Single-Error-Correcting Circuit**



**Statistics:** 41 inputs; 32 outputs; 202/546 gates; [bus translations](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499bus.html)

**Function:** c499 was found to be a single-error-correcting circuit as shown above. The 41 inputs are combined to form an 8-bit internal bus S, which then combines with 32 primary inputs to form the 32 primary outputs. The [boolean expressions defining S](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499sequ.html) form the [H matrix for a (40,32) Hamming code](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499hmatrix.html) [See C. L. Chen and M. Y. Hsiao. Error-Correcting Codes for Semiconductor Memory Applications: A State-of-the-Art Review. IBM Journal of Research & Development, vol. 28, pp. 124-134, March 1984]. If H\_ij (the element in row i and column j) is 1, then ID\_j (or IC\_j-32 if j > 31) is used in S\_i . Module M2 contains the necessary correcting logic, so c499 can correct single-bit errors; however, no error-detection logic is present. The S lines are formulated to generate a unique syndrome for each input line in error. The syndromes are the column vectors of H. If syndrome i is seen, output OD\_i is inverted. This is specified by the [32 output equations](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499oequ.html) realized by M2.

The c1355 circuit has the same overall function as c499; it differs in that all XOR primitives of c499 are expanded to their four-NAND-gate equivalents.

**Models:**

* [c499 ISCAS-85 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499.isc)
* [c499 Verilog hierarchical structural model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499.v)
* [c499/1355 Verilog hierarchical behavioral model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499b.v)
* [c499 complete gate-level tests](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c499.tests)
* [c1355 ISCAS-85 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c1355.isc)
* [c1355 Verilog hierarchical structural model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c1355.v)
* [c1355 complete gate-level tests](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c1355.tests)

**ISCAS-85 C499/C1355 32-Bit Single-Error Correcting Circuit**

**Bus Translations**

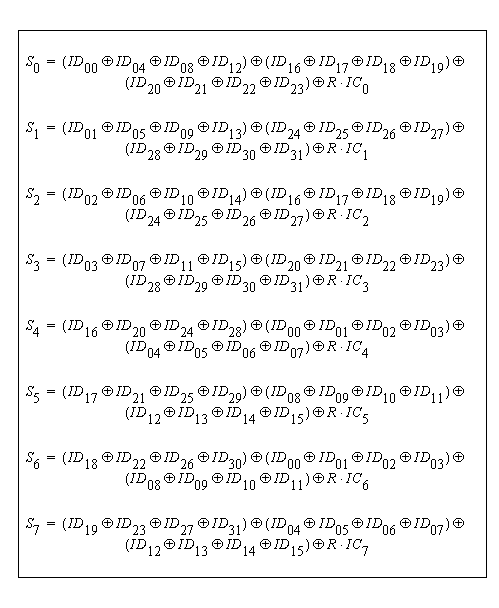
|  |  |  |
| --- | --- | --- |
| I/O buses | Function | ISCAS-85 Netlist numbers |
| ID[0:31] | Input data | 1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69,  73, 77, 81, 85, 89, 93, 97, 101, 105, 109, 113, 117, 121, 125 |
| IC[0:8] | Input code | 129, 130, 131, 132, 133, 134, 135, 136 |
| R | Read line | 137 |
| OD[0:31] | Corrected output data | 724-755 |

 **ISCAS-85 C499/C1355 32-Bit Single-Error Correcting Circuit**

**H matrix for a (40,32) Hamming code**

|  |  |  |
| --- | --- | --- |
|  | ID 00 - ID 31 | IC 0 - IC 8 |
| S7 - S0 | 1000 1000 1000 1000 1111 1111 0000 0000  0100 0100 0100 0100 0000 0000 1111 1111  0010 0010 0010 0010 1111 0000 1111 0000  0001 0001 0001 0001 0000 1111 0000 1111  1111 1111 0000 0000 1000 1000 1000 1000  0000 0000 1111 1111 0100 0100 0100 0100  1111 0000 1111 0000 0010 0010 0010 0010  0000 1111 0000 1111 0001 0001 0001 0001 | 1000 0000  0100 0000  0010 0000  0001 0000  0000 1000  0000 0100  0000 0010  0000 0001 |

**ISCAS-85 C499/C1355 Syndrome Equations**



**ISCAS-85 C499/C1355 Output Equations**

